Claims

What is claimed is:

1. A shift register device comprising:

a bit data input line along which bit data is to be shifted toward an output terminal;

latches in succession connected in series along said bit data input line and disposed between an input terminal and said output terminal, each latch capable of storing one bit of data;

transistor pass gates; and

control signal input lines connected to said transistor pass gates, each control signal input line operable to provide a control signal to one of said transistor pass gates to shift bit data to and from said latches along said bit data input line, wherein said control signals are applied in a staggered time pattern.

2. The shift register device of claim 1, wherein said bit data is shifted from a preceding latch to a succeeding latch.

3. The shift register device of claim 2, wherein said bit data is shifted from a preceding latch to a position external to said latches.

4. The shift register device of claim 3, wherein said bit data is shifted from a position external to said latches to a succeeding latch.

5. The shift register device according to claim 1, wherein said device is capable of storing four bits of data.

6. The shift register device according to claim 1, wherein said device includes four latches and four control signal input lines in succession.

7. The shift register device according to claim 6, wherein a control signal input line disposed last in succession is operable to provide a first control signal to a transistor pass gate disposed last in succession, a control signal input line disposed second to last in succession is operable to provide a second control signal to a transistor pass gate disposed second to last in succession, a control signal input line disposed third to last in succession is operable to provide a third control signal to a transistor pass gate disposed third to last in succession, and a control signal input line disposed fourth to last in succession is operable to provide a fourth control signal to a transistor pass gate disposed fourth to last in succession.

8. The shift register device according to claim 7, wherein said first control signal is provided before said second control signal, said second control signal is provided before said third control signal, and said third control signal is provided before said fourth control signal.

9. The shift register device of claim 7, wherein said transistor pass gate disposed last in succession is disposed between a latch disposed last in succession and a latch disposed second to last in succession.

10. The shift register device of claim 9, wherein said transistor pass gate disposed second to last in succession is disposed between said latch disposed second to last in succession and a latch disposed third to last in succession.

11. The shift register device of claim 10, wherein said transistor pass gate disposed third to last in succession is disposed between said latch disposed third to last in succession and a latch disposed fourth to last in succession.

12. The shift register device of claim 11, wherein said transistor pass gate disposed fourth to last in succession is disposed between said input terminal and said latch disposed fourth to last in succession.

13. The shift register device of claim 1, wherein said control signals are applied in succession beginning with application to a transistor pass gate disposed last in succession.

14. A method for driving a shift register device, said device comprising a bit data input line along which bit data is to be shifted toward an output terminal, a

succession of latches capable of storing one bit of data, said latches connected in series along said bit data input line and disposed between an input terminal and said output terminal, a succession of transistor pass gates, and a succession of clock signal input lines, each of said clock signal input lines connected to one of said transistor pass gates, each clock signal input line operable to provide an input clock signal to one of said transistor pass gates to shift bit data upon receipt of said input clock signal, comprising the steps of:

a) providing a first control signal to a transistor pass gate disposed last in succession via a control signal input line disposed last in succession;

b) shifting bit data from a latch disposed last in succession towards said output terminal upon providing said first control signal;

c) shifting bit data from a latch disposed second to last in succession to said latch disposed last in succession upon providing said first input clock signal;

d) providing a second control signal to a transistor pass gate disposed second to last in succession via a control signal input line disposed second to last in succession; and

e) shifting bit data from a latch disposed third to last in succession to said latch disposed second to last in succession upon providing said second control signal, wherein said first and second control signals are provided in a staggered time pattern and said first control signal is provided before said second control signal.

15. The method of claim 14, further comprising the steps of:

f) providing a third control signal to a transistor pass gate disposed third in succession via a control signal input line disposed third in succession;

g) shifting bit data from a latch disposed fourth to last in succession to said latch disposed third to last in succession upon providing said third control signal;

h) providing a fourth control signal to a transistor pass gate disposed fourth to last in succession via a control signal input line disposed fourth to last in succession; and

i) shifting input data to said latch disposed fourth to last in succession upon providing said fourth control signal, wherein said third and fourth control signals are provided in a staggered time pattern and said third control signal is provided before said fourth control signal.

16. The method according to claim 14, wherein steps a) to c) occur before steps d) and e).

17. The method according to claim 15, wherein steps a) to c) occur before steps d) and e) and steps f) and g) occur before steps h) and i) but after steps a) to e).

18. The method according to claim 15, further comprising repeating said steps a) to i).

19. A shift register device comprising:

latches in succession and connected in series along a bit data input line, each latch storing one bit of data; and

control signal input lines in succession connected to said latches, each line operable to provide a control signal to shift bit data along said bit data input line, wherein said control signals are applied in a staggered time pattern and in reverse succession.

20. The shift register device of claim 19, further comprising transistor pass gates connected to said control signal input lines, wherein said control signal input lines operate through said transistor pass gates.

21. The shift register device of claim 19, wherein said device includes four latches and four control signals.

22. The shift register device according to claim 21, further comprising four transistor pass gates, each transistor pass gate connected to one of said control signal input lines.